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09/666,054	09/20/2000	Sang Ho Lee	HI-017	5515

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EXAMINER	
MOORE, IAN N	

ART UNIT	PAPER NUMBER
2616	

DATE MAILED: 08/22/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/666,054	LEE, SANG HO	
	Examiner	Art Unit	
	Ian N. Moore	2616	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 June 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5,7-12,14,15,17,19,20,22-27,29,31-33,39,40,42 and 43* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1-5,7-12,14,15,17,19,20 and 22-25* is/are allowed.

6)☒ Claim(s) *26,27,29,31-33,39,40 and 42* is/are rejected.

7)☒ Claim(s) *43* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *9-20-2000* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. The drawing (**FIG. 3**) is objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference character(s) **not mentioned** in the description: 서보드 (at the upper left side of FIG. 3).

Corrected drawing sheets in compliance with 37 CFR 1.121(d), or amendment to the specification to add the reference character(s) in the description in compliance with 37 CFR 1.121(b) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 26,27,29,31-33, 39, 40 and 42 are rejected under 35 U.S.C. 103(a) as being unpatentable over (Uriu et al, hereinafter "Uriu", US Patent 5,301,184) in view of Blanc

(US006411599B1). Uriu discloses a control system for switching duplicated switch units in an ATM exchange.

With regard to claim 26, Uriu discloses a first system including switch 21a is operating as the active system (master board) and the second system including the switch 21 b is operating as the standby system (slave) (column 5, lines 26-39). Connections between individual components of the active system and the second system, as illustrated by Figure 3, (column 5, lines 14-26). Uriu further discloses a multiplexer or selector 27 connected to buffers 24a and 24b (connecting ports on master board and slave board) (column 5, lines 25-29). When the first system is switched from the active system to the standby system and the second system is switched from the standby system to the active system, the active system information bit (ATM cells state information / storing state information) "0" is written in each ATM cell applied to switch 21a (receiving/carrying ATM state information for the boards) and the active system indication bit (ATM cells state information / storing state information) "1" is written into each ATM cell applied to switch 21b (receiving ATM cells state information for the boards) (column 6, lines 16-23). The monitor unit 26a changes the active system indication bit related to first ATM cell stored in the VPI/VCI table 25a (virtual path / virtual channel) (column 6, lines 36-39).

Uriu does not disclose wherein signal lines for switching duplexing between the two boards, and wherein the signal lines connecting the ports on the master board and slave board bypass a bus. However, Blanc teaches wherein signal lines carry state information (see col. 3, line 10 to col. 4, line 9; control signals, watchdog or state information for ATM cells) for switching duplexing between the two boards (see FIG. 1, transmission through input to output port/pin connection 50i, 60, 40j between Switch Fabric left 10 and right 20; see col. 3, line 10 to

col. 4, line 36), and wherein the signal lines connecting the ports on the master board and slave board bypass a bus (see FIG. 1, avoiding/not-using/bypassing Bus/connection 32i, 33i, 34j, and/or 35j that couples switch fabric left and right; see col. 5, line 21-26; see col. 9, line 25-45) carrying ATM cells data for the boards (see col. 1, line 14-15; see col. 3, line 10-65; control signals, watchdog, and state information of ATM cells for the fabrics). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to provide input to output connections 50i, 60, 40 j between two switch fabrics by avoiding/not-using a cell bus/connection, as taught by Blanc in the system of Uriu, so that it would provide fault tolerant mechanisms providing high availability of the switching resources; see Blanc col. 2, line 1-12.

With regard to claim 27, Blanc al discloses wherein the number of signal lines is more than one (see FIG. 1, three lines/connections 50i, 60, and 40j between Switch Fabric left 10 and right 20; see col. 3, line 10 to col. 4, line 36). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to provide more than one input to output connections 50i, 60, 40 j between two switch fabrics, as taught by Blanc in the system of Uriu, for the same motivation as set forth above in claim 26.

With regard to claim 29, Uriu discloses when the first system is switched from the active system to the standby system and the second system is switched from the standby system to the active system, the active system information bit "0" is written in each ATM cell applied to switch 21a and the active system indication bit "1" is written into each ATM cell applied to switch 21b (column 6, lines 16-23). The writing of the active system information bit reads on applicant's reset signal. Blanc also discloses the state information includes a reset signal for resting the master board when the master boards switches to the standby state (see col. 3, line 10

to col. 4, line 9; control signals, watchdog or state information reset/change the state of the working/master/active fabric).

With regard to claim 31 and 32, Uriu discloses a first system including switch 21a is operating as the active system and the second system including the switch 21b is operating as the standby system (column 5, lines 26-39). Figure 3 illustrates the components of both the active and the second system. Specifically, the each system comprises a switch 21a and 21b (at least one port), a demultiplexer 22a and 22b, a first buffer 23a and 23b (memory), a second buffer 24a and 24b (memory), a VPI/VCI table 25a and 25b (memory), and a monitor unit 26a and 26b (controller) (column 5, lines 14-26). When the first system is switched from the active system to the standby system and the second system is switched from the standby system to the active system the active system information bit (state information) "0" is written in each ATM cell applied to switch 21a and the active system indication bit (state information) "1" is written into each ATM cell applied to switch 21 b (column 6, lines 16-23). The monitor unit 26a changes (updates) the active system indication bit (controls duplexing state) related to first ATM cell stored in the VPI/VCI table 25a. The second buffer 24a refers to the contents of VPI/VCI table 25a and prevents the first ATM cell from being written therein (column 6, lines 36-41).

With regard to claim 33, the combined system of Uriu and Blanc discloses a memory and Blanc disclose a memory which stores the state information and a controller controls based on state information as set forth above in claim 31. Blanc further discloses the slave board monitors changes in state information of the master board (see col. 3, line 10 to col. 4, line 9; monitoring and sending state information from right fabric to left fabric, or vice-versa.) Therefore, it would have been obvious to one having ordinary skill in the art at the time the

invention was made to provide monitoring and sending state information of a fabric to each other, as taught by Blanc in the system of Uriu, for the same motivation as set forth above in claim 26.

With regard to claim 39, Uriu discloses a first system including switch 21a is - operating as the active system (master board) and the second system including the switch 21 b is operating as the standby system (slave board) (column 5, lines 26-39). When the first system is switched from the active system to the standby system and the second system is switched from the standby system to the active system, the active system information bit (ATM cells state information / storing state information) "0" is written in each ATM cell applied to switch 21a (receiving state information) and the active system indication bit (ATM cells state information / storing state information) "1" is written into each ATM cell applied to switch 21b (receiving ATM cells state information) (column 6, lines 16-23). The monitor unit 26a changes the active system indication bit related to first ATM cell stored in the VPI/VCI table 25a (virtual path / virtual channel) (column 6, lines 36-39).

Uriu does not explicitly disclose transmitted through a pin-to-pin connection between the master and slave boards, said pin-to-pin connection bypassing a bus, which is coupled to the master and slave boards. However, Blanc teaches wherein the state information (see col. 3, line 10 to col. 4, line 9; control signals, watchdog or state information for ATM cells), is transmitted through a pin-to-pin connection between the master and slave boards (see FIG. 1, transmission through input to output port/pin connection 50i, 60, 40j between Switch Fabric left 10 and right 20; see col. 3, line 10 to col. 4, line 36), and said pin-to-pin connection bypassing a bus which is coupled to the master and slave boards (see FIG. 1, avoiding/not-using/bypassing

Bus/connection 32i, 33i, 34j, and/or 35j that couples switch fabric left and right; see col. 5, line 21-26; see col. 9, line 25-45) for carrying ATM cell information (see col. 1, line 14-15; see col. 3, line 10-65; control signals, watchdog, and state information of ATM cells). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to provide input to output connections 50i, 60, 40 j between two switch fabrics by avoiding/not-using a cell bus/connection, as taught by Blanc in the system of Uriu, so that it would provide fault tolerant mechanisms providing high availability of the switching resources; see Blanc col. 2, line 1-12.

With regard to claim 40, Uriu discloses a first system including switch 21a is operating as the active system (active state) and the second system including the switch 21b is operating as the standby system (standby state) (column 5, lines 26-39).

With regard to claim 42, Uriu discloses when the first system is switched from the active system to the standby system and the second system is switched from the standby system to the active system, the active system information bit "0" is written in each ATM cell applied to switch 21a and the active system indication bit "1" is written into each ATM cell applied to switch 21b (column 6, lines 16-23). The writing of the active system information bit reads on applicant's reset signal. Blanc et al discloses the switch fabric left 10 and right 20 are connected (connecting) to one another as illustrated by Figure 1 (see col. 3, line 10 to col. 4, line 36). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to provide connection between fabrics to send control signals, as taught by Blanc in the system of Uriu, for the same motivation as stated above in claim 39.

Allowable Subject Matter

4. Claims 1-5,7-12,14,15,17,19,20,22-25 are allowed.

5. Claim 43 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

6. Applicant's arguments with respect to claims 26,27,29,31-33,39,40, and 42 have been considered but are moot in view of the new ground(s) of rejection.

Regarding claim 39,40,42, the applicant argued that, "...Blanc does not tech or suggest transmitting state information through a "pin-to-pin connection bypassing a bus which is couple to the master and slave boards for carrying ATM cell information," where the state information "indicates a virtual path and virtual channel for determining an active state and a standby state of the slave board and the master board" as recited in claim 39..." in page 22, paragraph 1.

In response to applicant's argument, the examiner respectfully disagrees with the argument above.

Uriu discloses a virtual path and virtual channel for determining an active state and a standby state of the slave board and the master board, and transmitting/receiving/carrying ATM cells information as set forth in above rejection. Blanc teaches wherein the state information (**see col. 3, line 10 to col. 4, line 9; control signals, watchdog or state information for ATM cells**), is transmitted through a pin-to-pin connection between the master and slave boards (**see FIG. 1,**

transmission through input to output port/pin connection 50i, 60, 40j between Switch Fabric left 10 and right 20; see col. 3, line 10 to col. 4, line 36), and said pin-to-pin connection bypassing a bus which is coupled to the master and slave boards (**see FIG. 1, avoiding/not-using/bypassing Bus/connection 32i, 33i, 34j, and/or 35j that couples switch fabric left and right; see col. 5, line 21-26; see col. 9, line 25-45**) for carrying ATM cell information (**see col. 1, line 14-15; see col. 3, line 10-65; control signals, watchdog, and state information of ATM cells**). Thus, the combined system of Uriu and Blanc discloses the claimed invention.

In response to applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986). In this case, the rejection is based upon the combined system of Uriu and Blanc.

In view of the above, **the examiner respectfully disagrees** with applicant's argument and believes that the combination of references as set forth in the 103 rejections is proper.

Conclusion

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ian N. Moore whose telephone number is 571-272-3085. The examiner can normally be reached on 9:00 AM- 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Doris To can be reached on 571-272-7629. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

INM
8-8-06

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